REMARKS

Applicant gratefully acknowledges the Examiner's helpful comments (and those of his supervisor) made during a personal interview conducted on April 15, 2004. Present at the interview were the undersigned counsel, the Examiner and Supervisory Patent Examiner Nathan J. Flynn. During the interview, the Application (specifically claim 24) was discussed. The undersigned counsel presented proposed amendments to claim 24 which the Examiner and the Examiner's supervisor indicated would likely overcome the cited references.

Applicant notes that the claim amendments made herein are based on the proposed amendments to claim 24 discussed at the personal interview. Therefore, Applicant respectfully submits that the Examiner and his supervisor considered these claim amendments and have indicated that such amendments would overcome the cited references.

An Excess Claim Fee Payment Letter is submitted concurrently herewith to cover the cost of three (3) excess total claims.

Claims 5-27 are all the claims presently pending in the application. Claim 24 has been amended to further define the invention. Claims 25-27 have been added to claim additional features of the claimed invention.

Applicant gratefully acknowledges the Examiner's indication that claims 5-23 have been allowed. However, Applicant respectfully submits that all of the claims are allowable.

Claim 24 stands rejected upon informalities (e.g., 35 U.S.C. § 112, first paragraph). Claim 24 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Braun (U.S. Patent No. 6,110,277). Claim 24 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Kiyoku et al. (U.S. Patent No. 6,153,010).

These rejections are respectfully traversed in view of the following comments.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as recited in claim 24) is directed to a method of forming a group III nitride compound semiconductor device. The method includes forming amorphous portions of a substrate surface in a grid-shaped pattern by implanting ions in the substrate

surface, and forming a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous portions.

In conventional methods, a stress due to a thermal expansion coefficient difference between the group III nitride compound semiconductor layer and the substrate causes cracks in the group III nitride semiconductor layer (Application at page 1, lines 13-23).

The claimed invention, on the other hand, forms a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous portions (Application at page 17, line 1-page 18, line 19; Figures 9A-10). As a result, the group III nitride layers may be grown in small areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking (Application at page 2, line 17-page 3, line 4).

II. THE 35 USC §112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claim 24 is not enabled by the specification. Applicant submits, however, that claim 24 is fully enabled by the specification.

Specifically, Applicant would point out that the subject matter of claim 24 is fully described in the specification, for example, at page 17, line 1-page 18, line 19. In addition, Figures 9A, 9B and 10 provide clear illustrations of a group III nitride semiconductor device which may be made according to the method of claim 24.

In addition, the specification provides that the device-forming method such as a method for forming the group III nitride compound semiconductor layers 57, and the configuration of the device "are the same as those described in the previous embodiment" (Application at page 18, lines 18-19). Thus, the Application avoids being redundant by referring back to a first

embodiment (e.g., Application at page 11, lines 20-25) for a description of the method of forming the group III nitride semiconductor layers.

Therefore, Applicant submits that one of ordinary skill in the art would have no problem reading the specification and relying on the specification to perform the method of claim 24. Therefore, claim 24 is fully enabled by the specification.

Further, Applicant would point out that 35 USC 112, first paragraph requires only that one of ordinary skill in the art should be able to read the specification and make and use the claimed invention without **undue** experimentation. That is, it is not required that one of ordinary skill in the art can make and use the invention without **any** experimentation. Applicant submits that certainly one of ordinary skill in the art could read the present Application which is detailed and well-written and unambiguous, and based upon the Application, would be able to make and use the claimed invention without **undue** experimentation.

Therefore, Applicant submits that claim 24 is fully enabled by the specification. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Braun Reference

The Examiner alleges that Braun teaches the claimed invention of claim 24. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Braun.

Braun discloses a process for the fabrication on a monocrystal silicon substrate of epitaxial layers of a III-V nitride compound semiconductor. A parcel-like structure is created on the surface of a monocrystal silicon substrate. The silicon surface within the parcels is uncovered and the edges of the parcels are covered by a masking material. By means of epitaxial growth of the nitride compound semiconductor exclusively within the parcels on the silicon surface, local islands are created on whose edges the dislocations generated by the lattice mismatches are allegedly able to break down (Braun at Abstract).

Applicant submits, however, that Braun does not teach or suggest ""*forming a group III*

nitride compound semiconductor layer on said substrate surface such that a portion of said layer formed on said amorphous portions of said substrate surface has a different crystalline structure than a portion of said layer formed on portions of said substrate surface that are other than said amorphous portions", as recited in claim 24.

As noted above, unlike conventional methods, the claimed method forms a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous portions (Application at page 17, line 1-page 18, line 19; Figures 9A-10). As a result, the group III nitride layers may be grown in small areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking of the layer (Application at page 2, line 17-page 3, line 4).

Clearly, these features are not taught or suggested by Braun. Indeed, the Examiner attempts to rely on Figure 1 to support his allegations. However, Figure 1 merely illustrates a masking layer 20 which is formed on a substrate by oxidation, and a nitride compound semiconductor 30, 40 which is formed only on the substrate portions which are not covered by the masking layer 20.

That is, the nitride compound semiconductor 30, 40 is not even formed on significant portions (e.g., those covered by the mask 20) of the Braun substrate. Moreover, nowhere in this drawing, or anywhere else in Braun for that matter, is ion implantation either taught or suggested. Indeed, nowhere does Braun teach or suggest forming two portions of a nitride semiconductor layer (e.g.., on portions of a substrate having different crystalline structures) which are not connected. Thus, clearly, Braun is completely unrelated to the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Braun. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Kiyoku Reference

The Examiner alleges that Kiyoku teaches the claimed invention of claim 24. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Kiyoku.

Kiyoku discloses a method of growing nitride semiconductors which is intended to have very few crystal defects. In the method, a nitride semiconductor layer 71 is formed on an entire surface of a support member 10 made from a dissimilar substrate 11 and an underlayer 12 formed on the dissimilar substrate 11. A plurality of recesses portions 72 are formed in the nitride semiconductor layer 71. Growth control masks 73, 74 are formed on the upper surface portions of the nitride semiconductor layer 71. A nitride semiconductor crystal 75 is then grown in the recess portions (Kiyoku at col. 15, lines 4-65; col. 16, lines 31-37).

Applicant submits, however, that Kiyoku does not teach or suggest "*forming a group III nitride compound semiconductor layer on said substrate surface such that a portion of said layer formed on said amorphous portions of said substrate surface has a different crystalline structure than a portion of said layer formed on portions of said substrate surface that are other than said amorphous portions*", as recited in claim 24.

As noted above, unlike conventional methods, the claimed method forms a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous portions (Application at page 17, line 1-page 18, line 19; Figures 9A-10). As a result, the group III nitride layers may be grown in small areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking of the layer (Application at page 2, line 17-page 3, line 4).

Clearly, these features are not taught or suggested by Kiyoku. Indeed, Kiyoku is completely unrelated to the claimed invention.

The Examiner attempts to rely on Figure 7 (presumably Figure 7a) to support his position.

However, nowhere does this drawing (or anywhere else in Kiyoku for that matter) teach or suggest forming a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous portions.

Indeed, as noted above, Kiyoku merely discloses a method in which recesses 72 are formed in a nitride compound semiconductor layer 71, and a nitride compound semiconductor 75 is formed in the recesses 72 (Kiyoku at Figures 7A-7C). Clearly, this is completely unrelated to the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Kiyoku. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 5-27, all the claims pending and presently being examined in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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